AMENDMENTS TO THE CLAIMS:

This listing of the claims will replace all prior versions, and listings, of the claims in this application:

Listing of Claims:

1. (Currently Amended) A method comprising:

encoding, at an encoder, a plurality of N systematic bits across time and space into an encoded packet of size M bits, wherein encoding the plurality of N systematic bits comprises interleaving the plurality of N systematic bits;

determining a quality of at least a first channel from a feedback circuit;

channel interleaving the plurality of N systematic bits and parity bits corresponding to the N systematic bits;

dividing the encoded packet into a first transmission packet defining a first size M_1 bits that includes N_1 of the N systematic bits and a second transmission packet defining a second size M_2 bits that includes N_2 of the N systematic bits, wherein at least one of M_1 and N_1 is based on the determined quality of the first channel; and

transmitting in parallel the first transmission packet from a first antenna at a first rate at a first power modified by a first weight value over the first channel and the second transmission packet from a second antenna at a second rate that differs from the first rate and at the first power modified by a second weight value over a second channel, wherein M, M_1, M_2, N, N_1 and N_2 are all integers, M is greater than N, M is at least equal to M_1+M_2, and N is at least equal to N_1+N_2.

2. (Original) The method of claim 1 wherein dividing the encoded packet comprises maximizing a number N_1 of systematic bits in the first transmission packet.

3. (Original) The method of claim 2 wherein $N=N_1$ and $N_2=0$.

4. (Original) The method of claim 1 wherein $M_1=M_2$ and $N_1 \neq N_2$.

5. (Canceled)

6. (Previously Presented) The method of claim 1 wherein transmitting further comprises:

transmitting the second transmission packet from the second antenna over the second channel at a second power modified by a third weight value, and from the first antenna over the first channel at the second power modified by a fourth weight value.

7. (Original) The method of claim 1 wherein encoding a plurality of N systematic bits across time into an encoded packet of size M bits comprises interleaving over the M bits.

8. (Original) The method of claim 7 wherein encoding further comprises turbo encoding using a single turbo interleaver of size N prior to interleaving over the M bits.

9. (Original) The method of claim 1 wherein determining a quality of at least a first channel comprises determining a capacity of said first channel.

10.(Original) The method of claim 1 wherein determining a quality of at least a first channel comprises determining a quality of a second channel, and the values of M_1 and M_2 are determined from the quality of the first and second channels.

11. (Previously Presented) A device comprising:

an encoder having an input configured to receive a plurality of N systematic bits and an output configured to output a plurality of M bits, wherein M is greater than N, wherein the encoder is configured to encode the N systematic bits over time and to interleave the N systematic bits over space;

a channel feedback circuit configured to determine a channel characteristic of a first communication channel;

a demultiplexer having an input configured to receive an output of the channel feedback circuit, said demultiplexer configured to output in parallel a first portion M_1 of the M bits at a first output and a second portion M_2 of the M bits at a second output;

a channel interleaver disposed between the encoder and the demultiplexer and configured to channel interleave the N systematic bits and parity bits corresponding to the N systematic bits

and provide the channel interleaved N systematic bits and parity bits to the demultiplexer;

a first amplifier configured to increase a power of said first portion M_1 of the M bits to a first power prior to transmission from said first antenna;

a first antenna configured to transmit, at a first rate, said first portion M_1 of the M bits;

a second amplifier configured to increase a power of said second portion M_2 of the M bits to a second power prior to transmission from said second antenna; and

a second antenna configured to transmit, at a second rate that differs from the first rate, said second portion M_2 of the M bits; and

a first eigenvector block in series with the first output, said first eigenvector block configured to apply a first power weight factor to said first portion M_1 of the M bits prior to transmission from said first antenna and configured to apply a second power weight factor to said first portion M_1 of the M bits prior to transmission from said second antenna.

12-13. (Canceled)

14. (Previously Presented) The device of claim 11 wherein said first and second power weight factor are based on at least one of a size of said first M_1 and second M_2 portion and a channel quality of a first and second channel is provided by said channel feedback circuit, said first antenna configured to transmit over said first channel and said second antenna configured to transmit over said second channel.

15. (Previously Presented) The device of claim 11 further comprising:

a second eigenvector block in series with the second output, said second eigenvector block configured to apply a third weight factor to said second portion M_2 of the M bits prior to transmission from said second antenna and configured to apply a fourth power weight factor to said second portion M_2 of the M bits prior to transmission from said first antenna.

16. (Previously Presented) The device of claim 15 wherein said third and fourth power weight factors are based on at least one of a size of said first M_1 and second M_2 portion and a channel

quality of a first and second channel provided by said channel feedback circuit, said first antenna configured to transmit over said first channel and said second antenna configured to transmit over said second channel.

17. (Previously Presented) The device of claim 11 wherein said encoder comprises an interleaver of length N, the transmitter further comprising a channel interleaver of length M configured to receive the output of the encoder.

18. (Previously Presented) The device of claim 11 wherein the first M_1 and second M_2 portion are the same size and the systematic bits are not equally distributed among the first M_1 and second M_2 portion.

19. (Previously Presented) The device of claim 11 wherein said demultiplexer is configured to operate to maximize a number of systematic bits in the first portion M_1.

20. (Previously Presented) The device of claim 11 further comprising a first subpacket selector configured to receive the first output of the demultiplexer, configured to receive an output of the feedback circuit, and configured to provide a signal to the first antenna, said first subpacket selector configured to select and combine, into a first transmission packet that is transmitted over the first channel, the first portion M_1 and at least one additional subpacket from the first output of the demultiplexer, wherein a size of said first transmission packet is determined at least in part based on the output of channel feedback circuit.

21. (Previously Presented) A method comprising:

encoding a plurality of input bits across time and space;

based on a determined characteristic of at least a first channel, adaptively splitting the encoded input bits into a first subpacket defining a first subpacket size and a second subpacket defining a second subpacket size; and

transmitting the first subpacket at a first rate and at a first power over the first channel and the second subpacket at a second rate that differs from the first rate and at a second power that differs from the first power over a second channel, wherein the first and second powers are

determined using Lagrangian maximization with a total power constraint.

22. (Previously Presented) An apparatus comprising:

an encoder configured to encode a plurality of input bits over time and to interleave the input bits over space;

a demultiplexer configured to adaptively split the encoded plurality of bits into a first subpacket defining a first subpacket size and a second subpacket defining a second subpacket size;

a channel interleaver disposed between the encoder and the demultiplexer and configured to channel interleave the plurality of input bits and parity bits corresponding to the plurality of input bits;

a first antenna configured to transmit the first subpacket at a first rate and at a first power over a first channel; and

a second antenna configured to transmit the second subpacket at a second rate that differs from the first rate and at a second power that differs from the first power over a second channel, wherein the first and second powers are determined using Lagrangian maximization with a total power constraint.

23. (Previously Presented) The apparatus of claim 22 further comprising:

a channel feedback circuit configured to provide a channel characteristic of at least the first channel by which the demultiplexer adaptively splits the encoded plurality of bits.

24. (Previously Presented) The apparatus of claim 20 wherein the at least one additional subpacket comprises only parity bits.

25. (Previously Presented) The method of claim 1, further comprising:

channel interleaving the encoded packet of size M bits with other encoded packets;

and wherein dividing the encoded packet is after the channel interleaving.

26. (Previously Presented) The device of claim 11, wherein the further comprising a channel interleaver disposed between the encoder and the demultiplexer and configured to channel interleave the encoded packet of size M bits with other encoded packets.

27.(Previously Presented) The method of claim 21, further comprising channel interleaving the encoded input bits with other encoded packets prior to adaptively splitting the encoded input bits.

28. (Canceled).